

Remarks

Claims 1 - 18 are in the application, of which claims 11 - 18 were withdrawn as being directed to a nonelected invention. Accordingly, claims 1 - 10 are now under consideration.

Claims 1, 2, 3, 4 and 7 are amended herein. The specification is amended to update the related applications data. No new matter is introduced by any of the amendments, and entry thereof is requested.

Reconsideration of the application is requested, in view of the Remarks, following.

Applicants' invention is directed to multi-package modules comprising stacked lower and upper packages. Each package in the stack includes a die attached to, and electrically interconnected to, a substrate; and in each package the electrical interconnection is protected by encapsulation (wire bonded die) or by underfill (flip chip die). A lower side of the lower package substrate serves also as the lower surface of the module and, accordingly, the lower side of the lower package substrate is provided with second-level interconnect pads for mounting second-level interconnect solder balls. That is, the lower package substrate not only serves as a substrate for the lower package die and provides z-level electrical interconnection of the upper and lower packages within the module (by wire bond interconnect); but also serves to provide for second-level electrical interconnection of the module to circuitry of the environment in which it is used, such as a motherboard (by second-level interconnect solder balls).

Claim 1 is amended herein to emphasize the fact that, according to the invention, the lower package substrate serves as a substrate for the lower package die and provides for z-level interconnection between the packages in the module, and additionally provides for second-level interconnection of the module. Claim 1 is further amended to emphasize that the interconnections of the respective die and substrates are protected; claims 2, 3 and 4 recite protection of wire bond interconnections by encapsulation, and claim 7 recites protection of flip chip interconnection by underfill.

The points raised in the Office action will now be addressed.

Rejections under 35 U.S.C. § 102(b)

Claims 1 and 6 - 7 were rejected under 35 U.S.C. § 102(b) as being anticipated by Mori U.S. 5,903,049 ("Mori"). The Examiner stated:

Regarding claim 1, Mori (Fig. 1) discloses a multi-package module comprising stacked lower and upper packages 6b and 6a, each package including a die 1a/1b attached to a substrate 2a/2b (column 2, lines 41-47), wherein the upper and lower substrates 2a/2b are interconnected by wire bonding 7 (see rightmost wire 7).

Regarding claims 6-7, Mori's Fig. 1 further discloses that the package is a land grid array package and has flip chip interconnect of the die 1a/1b with the substrate 2a/2b.

Mori describes a "mounting substrate" (8 in Mori Fig. 1, *e.g.*). According to Mori, semiconductor packages 6b and 6a are mounted onto the mounting substrate 8; semiconductor packages 6b and 6a are electrically connected to each other by wire bonds connecting their respective wiring patterns; and both semiconductor package 6a and semiconductor package 6b are electrically connected to the mounting substrate 8 by wire bonds. Although Mori is silent as to second-level interconnection, Mori expressly teaches a "mounting substrate" for the module, in addition to the "element substrates" in the packages, and Mori expressly teaches mounting the packages onto and electrically interconnecting the packages to this additional mounting substrate. There is no teaching or suggestion in Mori of a multi-package module having stacked lower and upper packages, in which the substrate of the lower package both provides for z-level interconnection between the packages in the module, and provides for second-level interconnection of the module, as in Applicant's claimed invention.

These differences are significant, for a number of reasons. Generally, the cost of substrates contributes significantly to the overall cost of a package or module, and avoiding the use of an additional substrate can bring the cost the module down. Additionally, the thickness of the substrate contributes to the overall thickness of the package or module, and avoiding the use of an additional substrate can provide for a thinner module. Moreover, the footprint of the additional mounting substrate (and, concomitantly, the module footprint) as taught by Mori must necessarily be larger than the footprint of the largest one of the packages, to permit wire bonding the packages to the mounting substrate, while, according to applicant's invention, the footprint of the module can be the same as the footprint of the lower package.

Accordingly, Mori neither teaches nor suggests Applicants' invention as claimed, and the rejection of claim 1, and of claims 6 – 7 depending from claim 1, should now be withdrawn.

Rejections under 35 U.S.C. § 102(e)

Claims 1-2, 5-7 and 10 were rejected under 35 U.S.C. § 102(e) as being anticipated by Kikuma *et al.* U.S. 6,777,799 ("Kikuma"). The Examiner stated:

Regarding claims 1-2, Kikuma (Fig. 10) discloses a multi-package module comprising stacked lower and upper packages, the lower package including a die 74 attached to a substrate 76, wherein the upper substrate 76 and the lower substrate 26 are interconnected by wire bonding 84 and wherein at least one of the package has wire bond 82/86 interconnect of the die 74/72 with the substrate 76/26.

Regarding claims 5-6, Kikuma's Fig. 10 further discloses that the upper package is a land grid array package and the lower package is a ball grid array package.

Regarding claim 7, Kikuma (Fig. 17B) discloses a multi-package module comprised stacked lower and upper packages, the lower package including a die 72 attached to a substrate 26 and the upper package including a die 74 attached to a substrate 76, wherein the upper substrate 76 and lower substrate 26 are interconnected by wire bonding 86 and wherein each package has flip chip interconnect of the die 74/72 with the substrate 76/26 by the solder bumps.

Applicant disagrees with the Examiner's reading of Kikuma. Kikuma describes a stacked semiconductor device having a plurality of semiconductor chips stacked as one package, constructed by serially mounting semiconductor chips and wiring boards.

The package in Kikuma Fig. 10, for example, is constructed by production process shown in Figs. 12A to 12E. According to Kikuma, the lower semiconductor chip 72 is mounted on a flexible printed wiring board 26; then a flexible printed wiring board 76 is placed as a second substrate on a semiconductor chip 72; then a semiconductor chip 74 is secured onto the surface of the flexible printed wiring board 76; then (Fig. 12C) the various semiconductor chips and wiring boards are connected by wire bonds. And the package in Kikuma figure 17, for example, is constructed by serially mounting semiconductor chips and substrates.

There is no teaching or suggestion in Kikuma of a multi-package module constructed by stacking packages, and the rejections of claims 1, 2, 5, 7 and 10 as being anticipated by Kikuma should be withdrawn.

Rejections under 35 U.S.C. § 103(a)

Claims 2-3 and 10 were rejected under 35 U.S.C. § 103(a) for obviousness over Mori U.S. 5,903,049 ("Mori") in view of Applicant's Figs. 2 and 3. Applicant's Figs. 2 and 3 are relied upon as showing packages having wire bond interconnect, or flip chip interconnect, of the die and the substrate.

Claim 4 was rejected under 35 U.S.C. § 103(a) for obviousness over Mori U.S. 5,903,049 ("Mori") in view of Applicant's Figs. 2 and 3, and Lobianco U.S. 6,340,846 ("Lobianco"). Lobianco is relied upon as teaching partial encapsulation.

Claim 8 was rejected under 35 U.S.C. § 103(a) for obviousness over Mori U.S. 5,903,049 ("Mori") in view of Barrow U.S. 5,898,219 ("Barrow"). There was relied upon as teaching a heat spreader on the top surface of the package.

Claims 8-9 were rejected under 35 U.S.C. § 103(a) for obviousness over Mori U.S. 5,903,049 ("Mori") in view of Hoffman *et al.* U.S. 6,737,750 ("Hoffman"). Hoffman is relied upon as teaching a heat spreader formed on a top surface of a lower die, the Examiner arguing that it would have been obvious to form a heat spreader on a top surface of a lower package of Mori. Hoffman is for the relied upon as teaching an electromagnetic shield, the Examiner arguing that the heat spreader of Hoffman inherently functions as an electromagnetic field because it is connected to ground.

Applicant does not fully agree with the Examiner's reading of the secondary references, but these points need not be addressed here. As explained above, Mori fails to teach or suggest a multi-package module having stacked lower and upper packages, in which the substrate of the lower package both provides for z-level interconnection between the packages in the module, and provides for second-level interconnection of the module, as in Applicant's invention as claimed in claim 1. It is not shown how any of the secondary references, nor how any combination of the secondary references, supplies these features of applicants claimed invention and, accordingly, it is not shown how any combination of Mori with any of the secondary references makes applicant's invention has claimed in any of dependent claims 2 – 4 and 8 – 10.


Accordingly, the rejections for obviousness should now be withdrawn.

In view of the foregoing, all the claims now in the application are believed to be in condition for allowance, and action to that effect is respectfully requested

This Response is being filed within the third month following the three months' shortened statutory period set by the Examiner for response to the Office action and, accordingly, it is accompanied by a Petition for three months' extension of time and a fee or fee authorization therefor. In the event the Examiner may determine that additional fee[s] may be required in connection with the filing of this paper, petition is hereby made therefor, and the Commissioner is authorized to charge any additional fee (or to credit any overpayment) to Deposit Account No. 50-0869 (CPAC 1017-2).

If the Examiner determines that a conference would facilitate prosecution of this application, the Examiner is invited to telephone Applicants' representative, undersigned, at the telephone number set out below.

Respectfully submitted,

 *Reg. No. 33,407*

Bill Kennedy
Reg. No. 33,407

Haynes Beffel & Wolfeld LLP
P.O. Box 366
Half Moon Bay, CA 94019
Telephone: (650) 712-0340